



**GURU GOBIND SINGH INDRAPRASTHA UNIVERSITY,
EAST DELHI CAMPUS,
SURAJMAL VIHAR-110092**

Semester: 3rd			
Paper code: AIDS255/AIML255/IOT255	L	T/P	Credits
Subject: Digital Logic Design Lab	0	2	1
Marking Scheme			

1. Teachers Continuous Evaluation: As per university examination norms from time to time
2. End term Examination: As per university examination norms from time to time

INSTRUCTIONS TO EVALUATORS: Maximum Marks: As per university norms	
<ol style="list-style-type: none"> 1. This is the practical component of the corresponding theory paper. 2. The practical list shall be notified by the teacher in the first week of the class commencement under the intimation to the office of the HOD/ Institution in which the appear is being offered from the list of practicals below. 3. Instructors can add any other additional experiments over and above the mentioned in the experiment list which they think is important. 4. At least 8 experiments must be performed by the students. 	
Course Objectives:	
1.	To familiarize with the understanding of various aspects of designing real life applications through digital logic.
2.	Design and analysis of the digital circuits and systems.
Course Outcomes:	
CO1	Design an experiment to validate through hypothesis, a Boolean logic gates, truth table and circuit simulation.
CO2	Create circuits to solve real life problems via digital logic design.

CO/PO	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO1	2	2	2	2	1	-	-	-	-	-	-	1
CO2	2	2	2	2	1	1	1	1	1	1	1	1

LIST OF EXPERIMENTS:

1. a) Introduction to Digital Logic Trainer kits and their function.
b) Verify the truth table of Basic logic gates using their ICs.
c) Realize logic functions of NOT, AND, OR, EX-OR, EX-NOR with the help of universal gates-NAND and NOR Gates.
2. a) Verify De-Morgan's theorem for two variables using basic gates.
b) Realize Sum of Product (SOP) and Product of sum (POS) expressions using universal gates.
3. Realize Binary to Gray & Gray to Binary code converter and their truth table.
4. Design and test the Adder circuit.



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- a) Half Adder
 - b) Full Adder
 - c) Parallel Adder using 7483
5. Design and test the Subtractor circuit.
- a) Half Subtractor
 - b) Full subtractor
6. Design and test the Multiplexer circuit.
- a) 8:1 Multiplexer using IC 74151
 - b) 1:8 Demultiplexer circuit using IC 74138
7. Verify and test the Counter circuit.
- a) BCD Counter using ICs 7493
 - b) Ring counter using 7495
 - c) Johnson Ring Counter using 7495
8. Design and implement Comparator circuit.
- a) 1 bit comparator
 - b) 4 bit magnitude Comparator using 7485
9. Design and implement Encoder circuit.
- a) Decimal to BCD Encoder using IC 74147
 - b) Octal to Binary Encoder using IC 74148
10. Verify 2:4 Decoder using seven segment decoder and using ICs 7447.
11. Investigate the operation of various Flip-Flops using IC 7400, 7410.
- a) SR & Clocked Flip flop
 - b) D flip flop
 - c) T flip flop
 - d) JK flip flop
12. Realize Shift Register using ICs 7495.
- a) SISO (Serial in Serial out)
 - b) SIPO (Serial in Parallel out)
 - c) PIPO (Parallel in Parallel out)
 - d) PISO (Parallel in Serial out)